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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,004	10/28/2003	Lyle E. Adams	63479.0116	4256

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Matthew J. Booth & Associates, PLLC
P O BOX 50010
AUSTIN, TX 78763-0010

EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,004	ADAMS ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 17, 21, and 24-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 17, line 1, after "arbiters, the phrase: "one that couple to" appears to be a typing error. In line 3, after "target connection ports" the word "to" should be changed to – of --.

In claim 21, line 1, after "arbiters, the phrase: "one that couple to" appears to be a typing error. In line 3, after "target connection ports" the word "to" should be changed to – of --.

In claim 25, line 1, after "arbiters, the phrase: "one that couple to" appears to be a typing error. In line 3, after "target connection ports" the word "to" should be changed to – of --.

In claim 24, claim 24 is ambiguously constructed. As drafted, claim 24 is directed to an apparatus (an internal switching fabric). However, only steps (steps for providing) are recited in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 16-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Elabd (6,526,462).

As broadly drafted, these claims do not define any structure/step that differs from Elabd.

With regard to claim 16, Elabd discloses a System-on-Chip (SOC) interconnection apparatus (shown generally at Fig. 2), comprising: a single semiconductor integrated circuit (SOC, Fig. 2, for example) that includes one or more requestors with one or more requestor connection ports coupled thereto (CPU 4 or DSP 2, for example; it is clear that CPU 4 or DSP 2 include connection ports, and it is clear that dedicated memory buses 25a-25n and MT MMS having RCPU provides communications and connections between the masters and the targets) and one or more addressable targets with one or more target connection port coupled thereto (addressable targets 32/34, for example; it is clear that targets 32/34 include target connection ports, and it is clear that dedicated memory buses 25a-25n and MT MMS having RCPU provides communications and connections between the masters and the targets), wherein each said addressable target (32/34, for example) has a unique address space (one of the ten addresses of the memory space 86, see at least col. 11, line 35 to col. 12, line 7) and further comprises one or more of the following: resident

memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system (the addressable targets can be an internal or external memory 32/34); one or more decoder/router elements (the routing/switching RCPU and dedicated memory buses 25a-25n constitute internal switching fabric that that routes signals between said requesters and said addressable targets, the internal switching fabric comprises memory bus 25a-25n to decode the address of at least one addressable target, see at least col. 6, lines 15-17, and claim 17), wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map (memory mapping, see at least col. 11, line 35 to col. 12, line 7), and routes said request to said designated target (the routing/switching RCPU routes the request to a designated target). Further, it is clear that one of said one or more decoder/router elements of Elabd comprises one of the following: a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets (see Fig. 4 and description thereof, see also at

least col. 11, line 35 to col. 12, line 7). Still further, it is clear that additional requestors may be coupled to the internal switching fabric (the routing/switching RCPU and dedicated memory buses 25a-25n constitute internal switching fabric that routes signals between said requesters and said addressable targets, the internal switching fabric comprises memory bus 25a-25n to decode the address of at least one addressable target, see at least col. 6, lines 15-17, and claim 17) adding additional said requestor connection ports.

With regard to claim 17, it is clear that the internal switching fabric includes at least the arbiter 52 for arbitrating requests between the requestors and targets. See at least column 8, lines 15-37.

With regard to claim 18, as discussed above, it is clear that independently accessible requestor port and an independently accessible target port are provided in Elabd for a plurality of individual masters and individual targets.

With regard to claim 19, see discussion above. See also Figs. 4, 6 (a,b) and 12C, and description thereof. Note that MT MMS has the state machines.

With regard to claim 20, Elab discloses a method to manufacture an internal switching fabric within an System-On-Chip (SOC) that routes signal between requestors and addressable targets, comprising: coupling one or more target connection ports to one or more requestors (CPU 4 or DSP 2, for example; it is clear that CPU 4 or DSP 2 include connection ports, it is clear that dedicated memory buses 25a-25n and MT MMS having RCPU provides communications and connections between the masters and the targets; and it is also clear that requestor connection ports must be connected to

requestors); coupling one or more target connection ports to one or more addressable targets (addressable targets 32/34, for example; it is clear that targets 32/34 include target connection ports, it is clear that dedicated memory buses 25a-25n and MT MMS having RCPU provides communications and connections between the masters and the targets; and it is also clear that target connection ports must be connected to targets) wherein each said addressable target (32/34, for example) has a unique address space (one of the ten addresses of the memory space 86, see at least col. 11, line 35 to col. 12, line 7) and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system (the addressable targets can be an internal or external memory 32/34); coupling one or more decoder/router elements to said requestor connection ports and said target connection ports (it is clear that the decoder/router elements must be connected to the requestor connection ports and target connection port for routing/decoding information; further, the routing/switching RCPU and dedicated memory buses 25a-25n constitute internal switching fabric that that routes signals between said requesters and said addressable targets, the internal switching fabric comprises memory bus 25a-25n to decode the address of at least one addressable target, see at least col. 6, lines 15-17, and claim 17), wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map (memory mapping, see at least col. 11, line 35 to col. 12, line 7), and routes said request to said designated target (the routing/switching RCPU routes

the request to a designated target). Further, it is clear that one of said one or more decoder/router elements of Elabd comprises one of the following: a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets (see Fig. 4 and description thereof, see also at least col. 11, line 35 to col. 12, line 7). Still further, it is clear that additional requestors may be coupled to the internal switching fabric (the routing/switching RCPU and dedicated memory buses 25a-25n constitute internal switching fabric that routes signals between said requesters and said addressable targets, the internal switching fabric comprises memory bus 25a-25n to decode the address of at least one addressable target, see at least col. 6, lines 15-17, and claim 17) adding additional said requestor connection ports.

With regard to claims 21-23, see discussion above, since the subject matter presented in claims 21-23 has already been addressed.

With regard to claims 24-27, see discussion above, since the subject matter presented in claims 24-27 has already been addressed.

Response to Arguments

Applicants' arguments filed 5/12/2006 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The Elabd 102 Rejection:

Applicants argue that The claimed invention, on the other hand, describes a System-on-chip (SOC) interconnection method and apparatus that discloses an internal switching fabric that interconnects, via standard connection ports, one or more requestors and one or more addressable targets on a single semiconductor integrated

circuit. Each target has a unique address space, may or may not have internal arbitration, and may be resident (i.e., on-chip) memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, system, or subsystem, or any combination thereof. Targets and requestors are connected to the internal switching fabric using target and requestor connection ports. The internal switching fabric routes signals between requestors and targets using one or more decoder/router elements that determine which target is the designated target using an internal system memory map. Dedicated arbiters may be included for targets without internal arbitration. Since the amended claims include elements and limitations that are not shown, taught, or implied by the Elabd, Applicant therefore respectfully requests that the Examiner withdraw the claim rejections to claims 1-15 under 35 USC 102(e) as being anticipated by Elabd (US Pat. No. 6,526,462)."

Contrary to Applicants' argument, as set forth in the rejection, Elabd discloses a System-on-Chip (SOC) interconnection apparatus (shown generally at Fig. 2), comprising: a single semiconductor integrated circuit (SOC, Fig. 2, for example) that includes one or more requestors with one or more requestor connection ports coupled thereto (CPU 4 or DSP 2, for example; it is clear that CPU 4 or DSP 2 include connection ports, and it is clear that dedicated memory buses 25a-25n and MT MMS having RCPU provides communications and connections between the masters and the targets) and one or more addressable targets with one or more target connection port coupled thereto (addressable targets 32/34, for example; it is clear that targets 32/34 include target connection ports, and it is clear that dedicated memory buses 25a-25n

and MT MMS having RCPU provides communications and connections between the masters and the targets), wherein each said addressable target (32/34, for example) has a unique address space (one of the ten addresses of the memory space 86, see at least col. 11, line 35 to col. 12, line 7) and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system (the addressable targets can be an internal or external memory 32/34); one or more decoder/router elements (the routing/switching RCPU and dedicated memory buses 25a-25n constitute internal switching fabric that that routes signals between said requesters and said addressable targets, the internal switching fabric comprises memory bus 25a-25n to decode the address of at least one addressable target, see at least col. 6, lines 15-17, and claim 17), wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map (memory mapping, see at least col. 11, line 35 to col. 12, line 7), and routes said request to said designated target (the routing/switching RCPU routes the request to a designated target). Elabd further discloses that the internal switching fabric includes at least the arbiter 52 for arbitrating requests between the requestors and targets. See at least column 8, lines 15-37.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner